User's Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind Appendix A

Agilent Technologies E2466B Intel Pentium® Pro Preprocessor Interface

The Agilent Technologies E2466B Preprocessor Interface—At a Glance

The Agilent Technologies E2466B Pentium® Pro Preprocessor Interface provides a complete interface for state (transaction) or timing analysis between any Intel Pentium™ Pro target system and the Agilent Technologies logic analyzers listed below, in an Agilent Technologies 16500B mainframe. For inverse assembly, and accurate instruction execution tracing of up to four processors, the Agilent Technologies 16505A Prototype Analyzer is required. The Agilent Technologies E2467A APIC Bus Preprocessor Interface can also be used with the Pentium® Pro Preprocessor to provide simultaneous bus analysis.

For instruction disassembly, Branch Trace Messages must be enabled and caches must be disabled. This requires a Pentium ® Pro run-control tool and a 30-pin debug port on the target system.

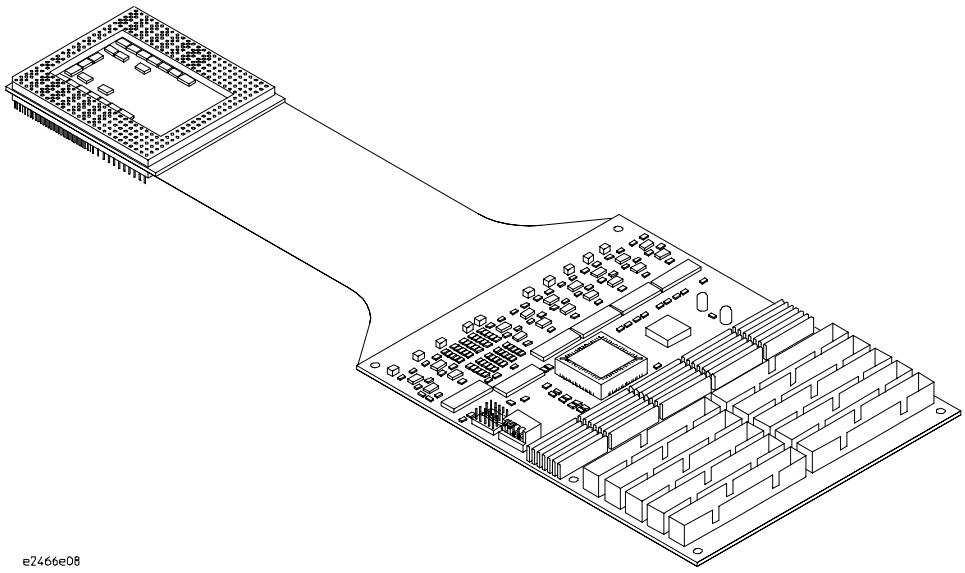
Logic Analyzer	Software Version	Channel Count	State Speed	Timing Speed	Memory Depth
16550A (two card)	v3.09	204	100 MHz	250 MHz	4 k states
16554A (three card)	v3.09	204	70 MHz	125 MHz	500 k states
16555A (three card)	v3.09	204	110 MHz	250 MHz	1 M states
16556A (three card)	v3.09	204	100 MHz	200 MHz	1 M states
Mainframe					
16500B Mainframe	v3.04				
Prototype Analyzer					
16505A Prototype Analyzer	A.01.22				

The preprocessor interface provides the physical connection between the target microprocessor and the logic analyzer. The Agilent Technologies 16500B configuration software on the flexible disk sets up the logic analyzer for compatibility with the preprocessor interface. The transaction tracker software allows you to obtain displays of the Pentium® Pro bus transactions.

An additional disk configures the Agilent Technologies 16505A Prototype Analyzer for Pentium® Pro inverse assembly. Note that transaction tracking is available with the logic analyzers, but inverse assembly is only available when the 16505A is also used.

For more information on the supported logic analyzers, the 16505A, or the microprocessor, refer to the appropriate reference manuals for those products.

Figure 1



Agilent Technologies E2466B Preprocessor Interface

In This Book

This book is the user's guide for the Agilent Technologies E2466B Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to set up and configure the preprocessor interface and logic analyzer for state or timing analysis.

Chapter 2 provides reference information on the logic analyzer format specification and symbols configured by the preprocessor interface software, and information about the transaction tracker files. It also contains information about the inverse assembler, available with the Agilent Technologies 16505A Prototype Analyzer.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

Contents

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the Agilent Technologies E2466B Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers. It also contains information on setting up the Agilent Technologies 16505A Prototype Analyzer for use with the Pentium® Pro preprocessor and using the Agilent Technologies E2467A APIC Bus Preprocessor Interface.

Before You Begin

This section lists the logic analyzers supported by the Agilent Technologies E2466B, and provides other information about the analyzers and the preprocessor.

Equipment Supplied

- The preprocessor interface circuit board.
- The transaction tracker software and configuration files, for the logic analyzer and Agilent Technologies 16500B mainframe, on a 3.5-inch disk. There are also Sample Trace files for all supported logic analyzers on the disk.
- Transaction tracker/inverse assembly software for the Agilent Technologies 16505A Prototype Analyzer on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

- The Agilent Technologies E2466B Pentium® Pro preprocessor interface, configuration files, and transaction tracker software.
- One of the logic analyzers listed in the table on page ii.
- An Agilent Technologies 16500B Logic Analysis Mainframe.

Additional Capabilities/Equipment Required

- In addition to basic transaction tracking, an Agilent Technologies 16505A Prototype Analyzer provides inverse assembly. This also greatly increases the analysis capability and performance. The Agilent Technologies E2466B Preprocessor Interface comes with software for the Agilent Technologies 16505A. Note that for instruction disassembly, Branch Trace Messages must be enabled and instruction caches must be disabled. This requires a Pentium® Pro run-control tool and a 30-pin debug port on the target system.
- For APIC Bus analysis, the Agilent Technologies E2467A APIC Bus Preprocessor Interface can be used with the Agilent Technologies E2466B.

Setting Up the Preprocessor Interface Hardware

Setting up for the preprocessor interface hardware consists of the following major steps:

1. Turn off the logic analyzer and the target system.

CAUTION

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

2. Set the State/Timing Mode switch and the Compacted/Expanded Clock Qualifier switch according to the type of analysis you wish to perform.
3. Install the preprocessor interface in the target system.
4. Connect the logic analyzer pods to the cable connectors of the preprocessor interface board.

To select the operating mode

Two switches on the preprocessor select the operating mode. The LEDs indicate the selected mode (see table 1).

The MODE switch selects either State or Timing mode. In State mode, the QUAL switch selects the clock qualifier to be either Compacted or Expanded. The QUAL switch has no effect in timing mode.

The Expanded clock qualifier acquires a state for every bus clock when there are transactions outstanding on the bus; no states are acquired when there are zero outstanding transactions.

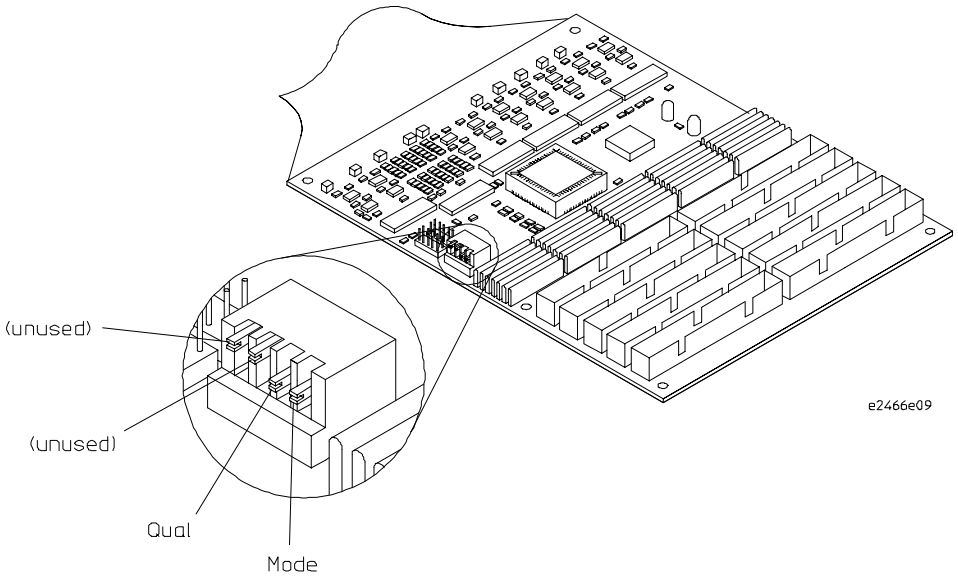
The Compacted clock qualifier maximizes the number of transactions captured and is generally preferred.

Refer to Chapter 3, section "Modes of Operation", for more details on the preprocessor operating modes and clock qualifiers.

Table 1. LED Indicators for Operating Mode

LEDs Lit	MODE Switch	QUAL Switch	Operating Mode/Clock Qualifier
Red only	Up	---	Timing
Red and Green	Down	Up	State with Expanded Clock Qualifier
Green only	Down	Down	State with Compacted Clock Qualifier

Figure 2



Switches for State/Timing Mode and Clock Qualifier

To connect to the target system

The microprocessor connector on the preprocessor will connect directly to a PGA socket on the target system.

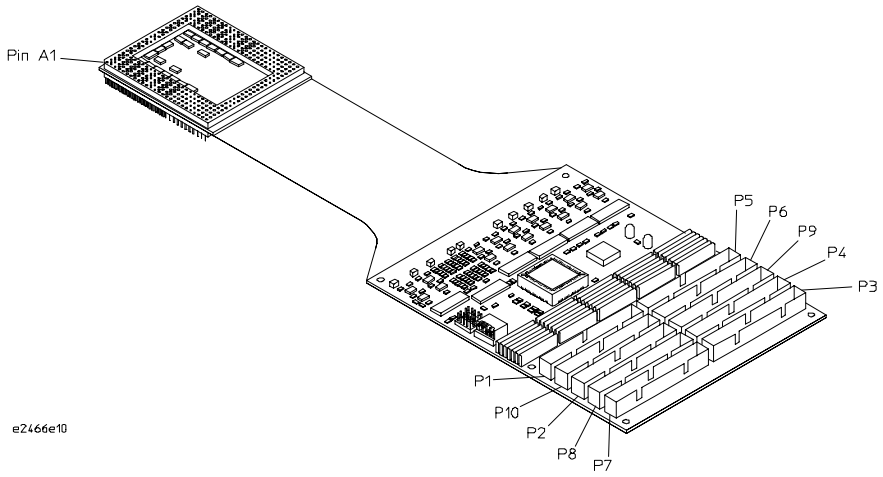
1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Remove the Pentium® Pro microprocessor from its socket on the target system and store it in a protected environment.

CAUTION

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 on the preprocessor interface, probe adapter assembly, and microprocessor prior to making any connection. Also, take care to align the preprocessor interface connector with the pins on the probe adapter assembly so that all pins are making contact.

3. Install the preprocessor interface into the PGA socket on the target system. Ensure that pin A1 is properly aligned (see figure below).
4. Plug the Pentium® Pro microprocessor into the socket on the preprocessor board. The socket on the preprocessor interface board is designed with low insertion force pins to allow insertion and removal with minimum force.

Figure 3

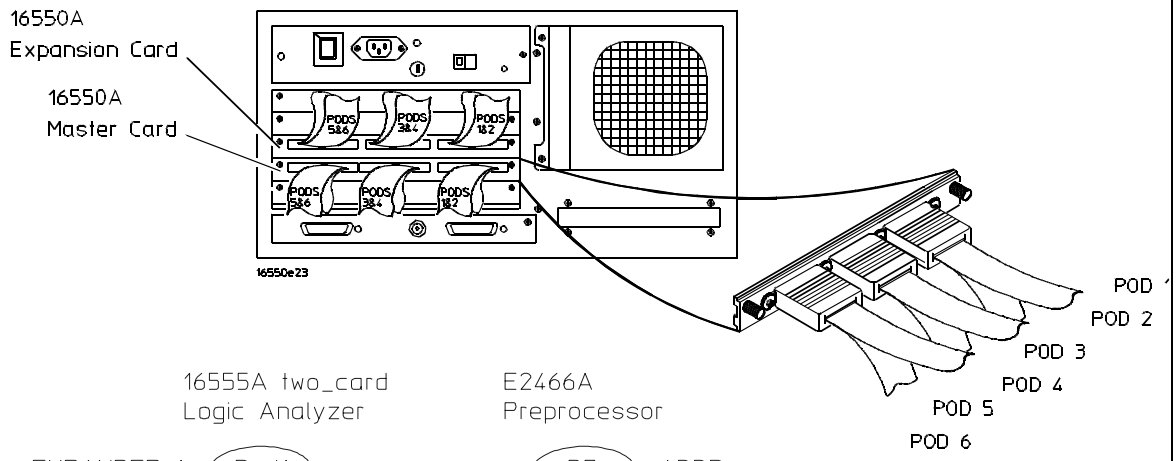


Pin A1 Location and Connector Numbers

CAUTION Support the Agilent Technologies E2466B PC board when connecting or disconnecting logic analyzer cables. This will help to prevent damage to the PC board and its components.

To connect to the 16550A two-card analyzer

Connect the logic analyzer pod cables to the preprocessor interface connectors according to this diagram.



16555A two_card Logic Analyzer		E2466A Preprocessor	
EXPANDER 1	Pod1	P7	ADDR
EXPANDER 1	Pod2	P8	ADDR
EXPANDER 1	Pod3	P9	ADDR_B
EXPANDER 1	Pod4	P10	ADDR_B
MASTER	Pod1	P1	STAT
MASTER	Pod2	P2	STAT
EXPANDER 2	Pod1	P3	DATA
EXPANDER 2	Pod2	P4	DATA
EXPANDER 2	Pod3	P5	DATA_B
EXPANDER 2	Pod4	P6	DATA_B

E2466B02

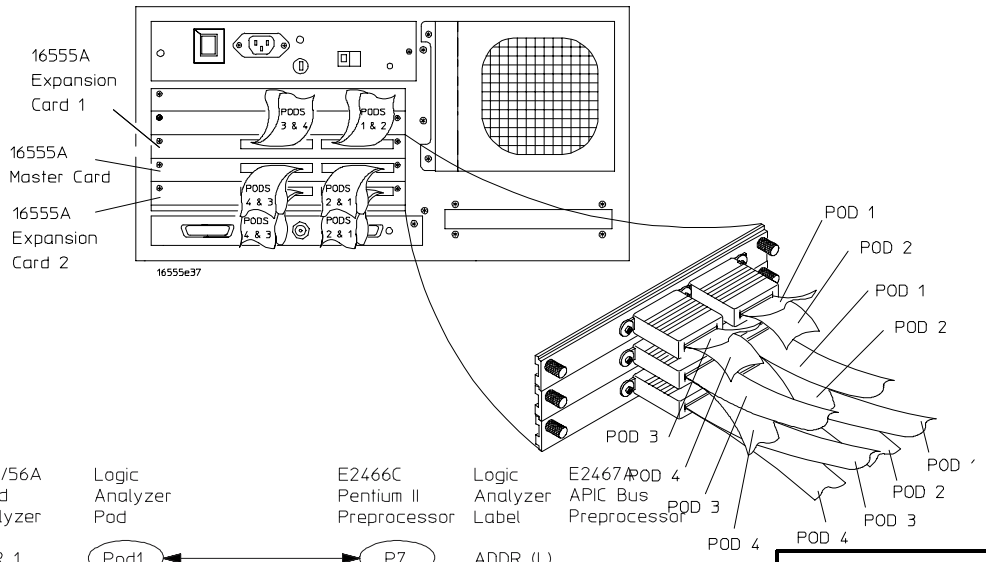
Configuration file

Use configuration file CP6C_1 for the two-card 16550A Logic Analyzer.

When using the E2467A APIC Bus Preprocessor Interface, the two pods marked unused are connected for APIC analysis. In this case, use configuration file CP6C_1A.

To connect to the 16554A/55A/56A analyzers

Connect the logic analyzer pod cables to the preprocessor interface connectors according to this diagram.



16554/55A/56A Three-card Logic Analyzer	Logic Analyzer Pod	E2466C Pentium II Preprocessor	Logic Analyzer Label	E2467A APIC Bus Preprocessor
EXPANDER 1	Pod1	P7	ADDR (L)	
EXPANDER 1	Pod2	P8	ADDR (H)	
EXPANDER 1	Pod3	P9	ADDR_B (L)	
EXPANDER 1	Pod4	P10	ADDR_B (H)	
MASTER	Pod1	J1	Clk↑ DATA (L)	
MASTER	Pod2	J2	DATA (H)	
MASTER	Pod3	P1	STAT (L) Clk↑	
MASTER	Pod4	P2	STAT (H)	
EXPANDER 2	Pod1	P3	DATA (L)	
EXPANDER 2	Pod2	P4	DATA (H)	
EXPANDER 2	Pod3	P5	DATA_B (L)	
EXPANDER 2	Pod4	P6	DATA_B (H)	

E2466B03

Configuration file

Use configuration file CP6C_2 for the 16554A/55A/56A Logic Analyzers.

When using the E2467A APIC Bus Preprocessor Interface, the two pods marked unused are connected for APIC analysis. In this case, use configuration file CP6C_2A.

To power up or power down

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

To protect the preprocessor interface when not in use

1. **Cover the socket assembly pins of the preprocessor interface with a conductive foam wafer or conductive plastic pin protector.**

   The socket assembly pins of the preprocessor interface were covered at the time of shipment with either a conductive foam wafer or conductive pin protector. If this device is not damaged, it may be reused repeatedly.

2. **Store the preprocessor interface in an antistatic bag or container.**

CAUTION

The socket assembly pins of the preprocessor interface should be covered with a conductive foam wafer or pin protector to protect the delicate gold plated pins of the assembly from damage due to impact. Covering the pins and properly storing the preprocessor interface also protects the active circuitry on the preprocessor interface from electrostatic discharge.

Setting Up the Preprocessor Interface Software

The preprocessor interface software consists of one Agilent Technologies 16500B logic analyzer disk and one Agilent Technologies 16505A Prototype Analyzer disk. The 16500B disk contains configuration files for the logic analyzer, and transaction tracker files. Inverse assembly is not available with the 16500B.

The 16505A disk contains both the transaction tracker and inverse assembler for the 16505A Prototype Analyzer. The 16505A is required for instruction disassembly (inverse assembly).

To load the 16500B logic analyzer files

1. The first time you set up the preprocessor interface, make a duplicate copy of the master disk.

   For information on duplicating disks, refer to the reference manual for your logic analyzer.
2. Ensure that the 16500B mainframe and the logic analyzer module have the required software version of the operating system.

   The version requirements are listed on page ii.
3. Insert the "16500B Logic Analyzer Configs" flexible disk in the disk drive of the 16500B.
4. Select the "System, Hard Disk" menu.
5. Create a directory on the logic analyzer using the command sequence "Make Directory, new directory name: <name>, Execute".
6. Select the "System, Flexible Disk" menu. Copy all files to the directory on the hard disk using the command sequence "Copy, file: *, to:\<name> on: Hard Disk, Execute".
7. Configure the menu to "Load" the analyzer configuration from the hard disk.
8. Select the appropriate module (such as "100/500 MHz LA") for the load.
9. Use the knob to select the appropriate configuration file. Note that there are different files if you are using the E2467A APIC Bus Preprocessor Interface together with the E2466B.

   Pentium® Pro Only

   - Select CP6C_1 if you are using the 16550A analyzer.
   - Select CP6C_2 if you are using the 16554A/55A/56A analyzer.

   Pentium® Pro and Agilent Technologies E2467A APIC Bus

   - Select CP6C_1A if you are using the 16550A analyzer.
   - Select CP6C_2A if you are using the 16554A/55A/56A analyzer.
10. Execute the load operation to load the file into the logic analyzer.

    The logic analyzer is configured for Pentium® Pro analysis by loading the appropriate configuration file. Loading this file also automatically loads the IAP6B2E transaction tracker file.

    For more information about the transaction tracker, refer to Chapter 2.

To load the 16505A Prototype Analyzer files

The Agilent Technologies 16505A Prototype Analyzer is required for inverse assembly. It also greatly increases both the performance and the capability of the analyzer user interface. To set up the prototype analyzer:

1. If you have not already done so, load the logic analyzer files as described in the previous section.

   The 16500B files must be loaded first for the 16505A to configure properly.

2. Connect the 16505A to the 165000B. Power up the 16500B first, then power up the 16505A.

   For information on connecting the 16505A, refer to the *Agilent Technologies 16505A Installation Guide*.

3. Ensure that the 16505A has software version A.01.22 or greater.

   You may check the 16505A system version from a running session. In the Main window, click Help, then click "On Version...".

4. Install the 16505A software for the Pentium® Pro.

   Place the "16505A Prototype Analyzer Disk" flexible disk in the disk drive of the 16505A. In the Session Manager window, select the **`Update`** button. The window should display

   Filegroup: pp_pent_pro
   Version: A.01.22.

   Click on Update/Install and respond to the question by clicking on OK. Wait for the Information dialog to confirm a successful installation. Click on OK to acknowledge, and Close the Update/Install window.

5. Load the configuration file.

   Start a session from the Session Manager window. When the main 16505A window opens, click on File in the top menu bar to get a pull-down menu, then click on "Load 16500 Files...". Change to the appropriate directory and load the appropriate file, either CP6C_1 or CP6C_2 (for Pentium® Pro only analysis) or CP6C_1A or CP6C_2A (for Pentium® Pro and E2467A APIC Bus analysis). Next, drag and drop a logic analyzer Instrument (either a 2-card 16550A or a 3-card 16554A/55A/56A) into the workspace area. Next, drag and drop a Listing Display on the "Pent Pro" Instrument icon in the workspace. Double click on the Listing icon to open the Listing window and verify that the label "Pentium Pro Inverse Assembly" appears.

To set up the preprocessor interface for timing

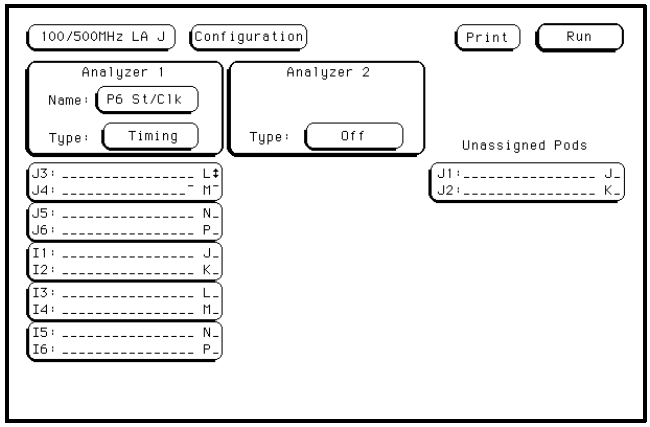
The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Configure the Agilent Technologies E2466B for timing analysis by setting the MODE switch to the "Up" position. Only the Red LED should be lit.
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field for the analyzer and select Timing.

Example

The following figure shows the Configuration Menu display for the Agilent Technologies 16550A logic analyzer:

Figure 4



Configuration Menu

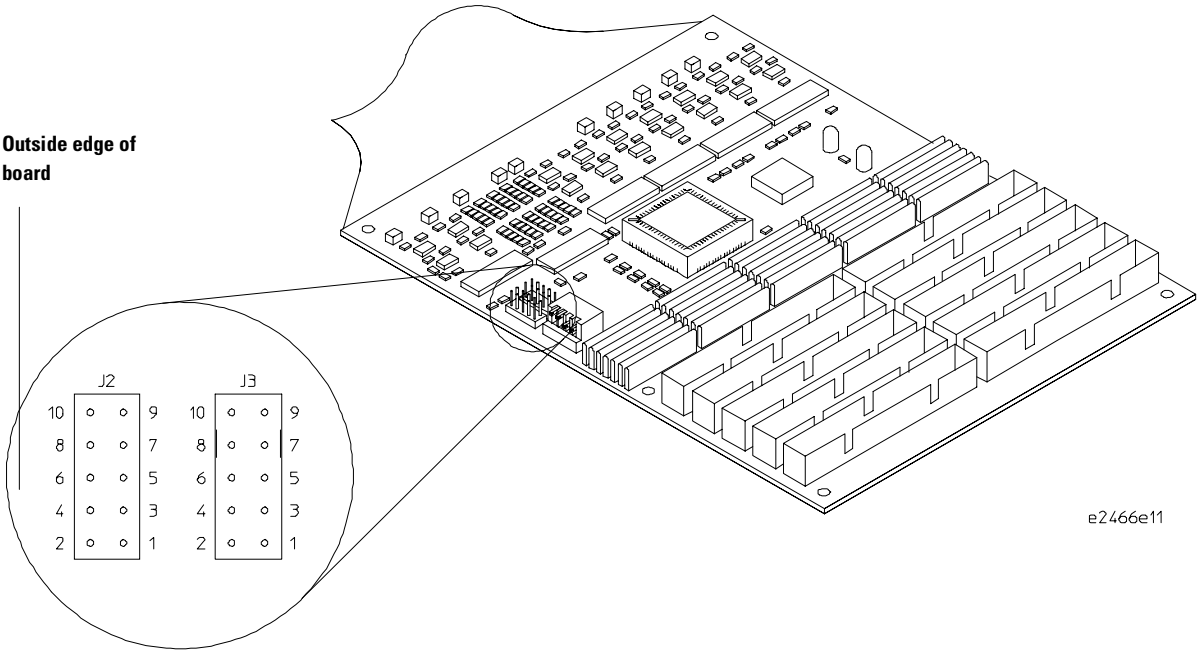
To connect to the APIC and JTAG signals

The APIC and JTAG signals are routed to headers J2 and J3, located next to the mode switches. These signals can be probed using the GP [General Purpose] probes that are shipped with your logic analyzer. Figure 5 shows the location of the headers. Table 2 shows the signals that are located on the pins of each header. These signals, with the exception of "lreset", are buffered versions of the Pentium® Pro bus signals; they are not latched by the bus clock. The special signal "lreset" is an inverted version of the P6 RESET# signal and is latched by the bus clock.

> Do not attempt to use the JTAG header as a run-control interface. This header is only capable of monitoring JTAG activity.

The APIC signals can be connected to the Agilent Technologies E2467A APIC Bus Preprocessor Interface.

Figure 5



Pin locations for APIC and JTAG signals

Table 2. Pin locations for APIC and JTAG signals

J2 (APIC)				J3 (JTAG)			
Pin #	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**
10	n/c	9	n/c	10	GND	9	TRST#
8	n/c	7	Ireset	8	GND	7	TDO
6	GND	5	PICD1#	6	GND	5	TDI
4	GND	3	PICD0#	4	GND	3	TMS
2	GND	1	PICCLK	2	GND	1	TCK

2

Analyzing the Intel Pentium® Pro

Analyzing the Intel Pentium® Pro

This chapter describes how to display configuration information and preprocessor interface data, gives label and symbol encodings for the status field, and provides information about the transaction tracker (for use with the Agilent Technologies 16500B or the 16505A) and the inverse assembler (available only with the Agilent Technologies 16505A).

Displaying Information

This section describes how to display logic analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To display the format specification

- **Select the format specification menu for your logic analyzer.**

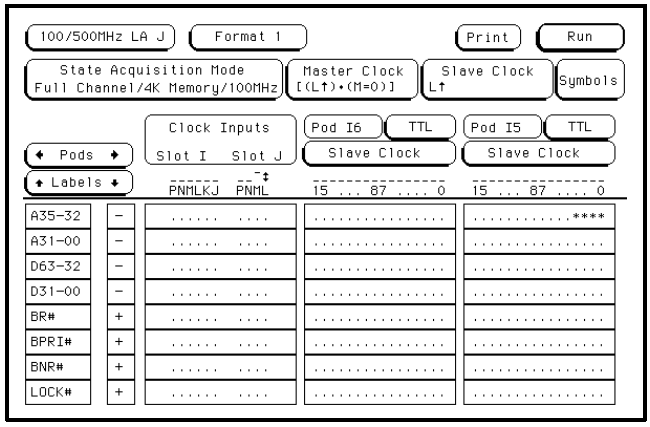
  The Pentium® Pro configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor bus.

  Chapter 3 of this guide contains a table that lists the signals for the Pentium® Pro processor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

Example

The format specification display shown in the following figure is from the Agilent Technologies 16550A logic analyzer. Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

Figure 6



Logic Analyzer Format Specification

To display the configuration symbols

- **Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.**

  The Agilent Technologies E2466B configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels simplify triggering on specific Pentium® Pro cycles. The label base in the symbols menu is set to hexadecimal to conserve display space.

  All Pentium® Pro signals are routed to the logic analyzer probe headers or to extra headers. Labels that contain all lower case letters are signals that are created by the preprocessor hardware; these signals are described more fully in chapter 3, "Modes of Operation". Labels that begin with an uppercase letter and have lower case letters within them are signals that combine preprocessor generated signals and Pentium® Pro signals.

The first of the following tables describes the Pentium® Pro signals that are captured by the preprocessor. The second table lists the label and symbol encodings defined by the logic analyzer configuration software.

Note 1

Under the heading "Polarity", negative means that the logic analyzer inverts the signal. Positive means that the logic analyzer does not invert the signal.

Note 2

Signals marked with an asterisk "*" contain phase qualifiers in their labels. When the symbol base is selected, these signals will only be displayed as valid if they are in a valid phase.

Table 3. Signal/Label List

Label Name	Polarity	Number of bits	Description	
Address/Data Bus Signals				
A35-32	negative	4	Address bus bits 35:32	
A31-00	negative	32	Address bus bits 31:00	
D63-32	negative	32	Data bus bits 63:32	
D31-00	negative	32	Data bus bits 31:00	
Arbitration Phase Signals				
BR#	positive	4	Symmetric Agent Bus request signals	
BPRI#	positive	1	Priority Agent Bus Request signal	
BNR#	positive	1	Block Next Request signal	
LOCK#	positive	1	Bus Lock signal	
Request Phase Signals				
ADS#	positive	1	Address Strobe	
REQ#	positive	5	Request Command	
Request Phase A Signals				
REQa#	positive	6	Request Command (Phase A)	* (see note 2)
ASZ#	positive	5	Memory Address-Space Size	* (see note 2)
W/R#	positive	4	Write/Read signal	* (see note 2)
D/C#	positive	4	Data/Code signal	* (see note 2)
W/WB#	positive	4	Write/Writeback signal	* (see note 2)
RplyID	negative	13	Deferred Reply Transaction ID	* (see note 2)

Table 3. Signal/Label List (Cont.)

Label Name	Polarity	Number of bits	Description	
Request Phase B Signals				
REQb#	positive	6	Request Command (Phase B)	* (see note 2)
DSZ#	positive	3	Data Size	* (see note 2)
LEN#	positive	3	Data Length	* (see note 2)
ATTR#	positive	9	Attribute signals	* (see note 2)
DID#	positive	9	Deferred Identifier signals	* (see note 2)
AgType	negative	2	Agent Type	* (see note 2)
AgntID	negative	4	Agent ID	* (see note 2)
TrnsID	negative	5	Transaction ID	* (see note 2)
BE#	positive	9	Byte Enables	* (see note 2)
EXF#	positive	6	Extended Function signals	* (see note 2)
SMMEM#	positive	2	System Management Mode Memory	* (see note 2)
SPLCK#	positive	2	Split Lock	* (see note 2)
DEN#	positive	2	Defer Enable	* (see note 2)
Error Phase Signals				
AERR#	positive	1	Address Parity Error signal	
Error	negative	2	Address Parity Error result	
Snoop Phase Signals				
HIT#	positive	1	Snoop Hit signal	
HITM#	positive	1	Snoop Hit Modified signal	
Snoop	negative	3	Snoop Result	
DEFER#	positive	1	Defer signal	
Response Phase Signals				
RS#	positive	3	Response Status	
TRDY#	positive	1	Target Ready signal	
Data Phase Signals				
DRDY#	positive	1	Data Ready signal	
DBSY#	positive	1	Data Bus Busy signal	

Table 3. Signal/Label List (Cont.)

Label Name	Polarity	Number of bits	Description
Parity Signals			
RSP#	positive	1	Response Parity signal
RP#	positive	1	Request Parity signal
DEP#	positive	8	Data bus ECC/Parity signals
AP#	positive	2	Address Parity signals
Execution Control Signals			
BCLK	positive	1	Bus Clock signal
INIT#	positive	1	Initialization signal
RESET#	positive	1	Reset signal
FLUSH#	positive	1	Flush signal
STPCK#	positive	1	Stop Clock signal
LINT	positive	2	Local Interrupt signals
NMI	positive	1	Non-maskable Interrupt signal
INTR	positive	1	Interrupt Request signal
SMI#	positive	1	System Management Interrupt signal
Error Signals			
BINIT#	positive	1	Bus Initialization signal
BERR#	positive	1	Bus Error signal
IERR#	positive	1	Internal Error signal
FRCERR	positive	1	Functional Redundancy Check Error signal
PC Compatibility Signals			
A20M#	positive	1	Address bit 20 Mask signal
FERR#	positive	1	Floating-point Error signal
IGNNE#	positive	1	Ignore Numeric Error signal

Table 3. Signal/Label List (Cont.)

Label Name	Polarity	Number of bits	Description
System Diagnostic Support signals			
PREQ#	positive	1	Probe Request signal
PRDY#	positive	1	Probe Ready signal
BP3#	positive	1	Breakpoint signal
BP2#	positive	1	Breakpoint signal
BPM1#	positive	1	Breakpoint and Performance Monitor signal
BPM0#	positive	1	Breakpoint and Performance Monitor signal
Transaction Tracker (Inverse Assembler) interface labels			
ADDR_B	negative	32	A35:32# and other status signals
ADDR	negative	32	A31:00# signals
DATA_B	negative	32	D63:32# signals
DATA	negative	32	D31:00# signals
STAT	negative	32	Status signals
STAT_0	negative	32	Same as STAT
STAT_1	negative	32	Same as ADDR_B
Preprocessor generated signals			
rcnt	negative	4	Request Count
scnt	negative	4	Snoop Count
bqual#	positive	1	Request Phase B Qualifier signal
equal#	positive	1	Error Phase Qualifier signal
squal#	positive	1	Snoop Phase Qualifier signal
cqual#	positive	1	Clock Qualifier signal
mqual#	positive	1	Probe Mode Qualifier signal
config	positive	1	Operating Modes Configuration serial channel

The following table lists the label and symbol encodings defined by the logic analyzer configuration software.

Note 3 The base is shown with the values in binary.

Table 4. Pentium® Pro Symbols

Signal	Symbol	Value
BPRI#	"Pri Agnt Bus Req" " --- "	0 1
BNR#	"Block Next Req" " --- "	0 1
LOCK#	"Bus Locked" " --- "	0 1
ADS#	"Request A" " --- "	0 1
REQa# = ADS#, REQ4:0#	"Deferred Reply " "RSVD (Ignore) " "Int Ack/Special " "Branch Trace Msg" "I/O Read " "I/O Write " "RSVD (Ignore) 2 " "Mem Read & Inval" "RSVD (Mem Write)" "Mem Read Data " "Mem Read Code " "Mem Write " "Mem Writeback " "RESERVED " " --- "	0 11111 0 11110 0 10111 0 10110 0 01111 0 01110 0 0011x 0 xx101 0 xx100 0 xx001 0 xx011 0 xx000 0 xx010 0 xxxxx 1 xxxxx
ASZ# = ADS#, REQ4:1#	"32 bit" "36 bit" "RESRVD" "32 bit" "36 bit" "RESRVD" " --- " " --- "	0 1110 0 1010 0 0x10 0 110x 0 100x 0 0x0x 0 xxxx 1 xxxx

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
W/R# = ADS#, REQ2:0#	"Write" "Read " "Write" "Read " " --- " " --- "	0 100 0 101 0 0x0 0 0x1 0 xxx 1 xxx
D/C# = ADS#, REQ2:0#	"Data" "Code" " ---" " ---"	0 001 0 011 0 xxx 1 xxx
W/WB# = ADS#, REQ2:0#	"Write " "Wrtback" " --- " " --- "	0 000 0 010 0 xxx 1 xxx
DSZ# = REQb4:3#, bqual#	"64 bit" "RESRVD" " --- "	11 0 xx 0 xx 1
LEN# = REQb1:0#, bqual#	"partial" "16bytes" "line " "RESRVED" " --- "	11 0 10 0 01 0 xx 0 xx 1
HIT#	"Hit" "---"	0 1
HITM#	"Hit Mod" " --- "	0 1
Snoop = HIT# ,HITM#, squal#	"Clean " "Modified" "Share " "Stall " " --- "	00 1 01 1 10 1 11 1 XX 0
DEFER#	"Defer" " --- "	0 1

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
ATTR# = A31:24#, bqual#	"UC " "USWC" "WT " "WP " "WB " "resv" "--- "	xxxx xx111 0 xxxx xx011 0 xxxx xx010 0 xxxx xx001 0 xxxx xx000 0 xxxx xxxxx 0 xxxx xxxxx 1
AgType = A23#, bqual#	"Symmetric" "Priority " " --- "	0 1 1 1 x 0
AgntID = A22:20#, bqual#	"Agnt 0" "Agnt 1" "Agnt 2" "Agnt 3" "Agnt 4" "Agnt 5" "Agnt 6" "Agnt 7" " --- "	000 1 001 1 010 1 011 1 100 1 101 1 110 1 111 1 xxx 0
TrnsID = A19:16#, bqual#	"Trans 0" "Trans 1" "Trans 2" "Trans 3" "Trans 4" "Trans 5" "Trans 6" "Trans 7" "Trans 8" "Trans 9" "Trans A" "Trans B" "Trans C" "Trans D" "Trans E" "Trans F" " --- "	0000 1 0001 1 0010 1 0011 1 0100 1 0101 1 0110 1 0111 1 1000 1 1001 1 1010 1 1011 1 1100 1 1101 1 1110 1 1111 1 xxxx 0

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
RplyID = A23#, A21:16#, ADS#, REQ4:0# (13 bits)	"sym ag0 tr0"	0000000 1 00000
	"sym ag0 tr1"	0000001 1 00000
	"sym ag0 tr2"	0000010 1 00000
	"sym ag0 tr3"	0000011 1 00000
	"sym ag0 tr4"	0000100 1 00000
	"sym ag0 tr5"	0000101 1 00000
	"sym ag0 tr6"	0000110 1 00000
	"sym ag0 tr7"	0000111 1 00000
	"sym ag0 tr8"	0001000 1 00000
	"sym ag0 tr9"	0001001 1 00000
	"sym ag0 trA"	0001010 1 00000
	"sym ag0 trB"	0001011 1 00000
	"sym ag0 trC"	0001100 1 00000
	"sym ag0 trD"	0001101 1 00000
	"sym ag0 trE"	0001110 1 00000
	"sym ag0 trF"	0001111 1 00000
	"sym ag1 tr0"	0010000 1 00000
	"sym ag1 tr1"	0010001 1 00000
	"sym ag1 tr2"	0010010 1 00000
	"sym ag1 tr3"	0010011 1 00000
	"sym ag1 tr4"	0010100 1 00000
	"sym ag1 tr5"	0010101 1 00000
	"sym ag1 tr6"	0010110 1 00000
	"sym ag1 tr7"	0010111 1 00000
	"sym ag1 tr8"	0011000 1 00000
	"sym ag1 tr9"	0011001 1 00000
	"sym ag1 trA"	0011010 1 00000
	"sym ag1 trB"	0011011 1 00000
	"sym ag1 trC"	0011100 1 00000
	"sym ag1 trD"	0011101 1 00000
	"sym ag1 trE"	0011110 1 00000
	"sym ag1 trF"	0011111 1 00000

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
RplyID = A23#, A21:16#, ADS#, REQ4:0# (13 bits) (continued)	"sym ag2 tr0"	0100000 1 00000
	"sym ag2 tr1"	0100001 1 00000
	"sym ag2 tr2"	0100010 1 00000
	"sym ag2 tr3"	0100011 1 00000
	"sym ag2 tr4"	0100100 1 00000
	"sym ag2 tr5"	0100101 1 00000
	"sym ag2 tr6"	0100110 1 00000
	"sym ag2 tr7"	0100111 1 00000
	"sym ag2 tr8"	0101000 1 00000
	"sym ag2 tr9"	0101001 1 00000
	"sym ag2 trA"	0101010 1 00000
	"sym ag2 trB"	0101011 1 00000
	"sym ag2 trC"	0101100 1 00000
	"sym ag2 trD"	0101101 1 00000
	"sym ag2 trE"	0101110 1 00000
	"sym ag2 trF"	0101111 1 00000
	"sym ag3 tr0"	0110000 1 00000
	"sym ag3 tr1"	0110001 1 00000
	"sym ag3 tr2"	0110010 1 00000
	"sym ag3 tr3"	0110011 1 00000
	"sym ag3 tr4"	0110100 1 00000
	"sym ag3 tr5"	0110101 1 00000
	"sym ag3 tr6"	0110110 1 00000
	"sym ag3 tr7"	0110111 1 00000
	"sym ag3 tr8"	0111000 1 00000
	"sym ag3 tr9"	0111001 1 00000
	"sym ag3 trA"	0111010 1 00000
	"sym ag3 trB"	0111011 1 00000
	"sym ag3 trC"	0111100 1 00000
	"sym ag3 trD"	0111101 1 00000
	"sym ag3 trE"	0111110 1 00000
	"sym ag3 trF"	0111111 1 00000

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
RplyID = A23#, A21:16#, ADS#, REQ4:0# (13 bits) (continued)	"pri ag0 tr0" "pri ag0 tr1" "pri ag0 tr2" "pri ag0 tr3" "pri ag0 tr4" "pri ag0 tr5" "pri ag0 tr6" "pri ag0 tr7" "pri ag0 tr8" "pri ag0 tr9" "pri ag0 trA" "pri ag0 trB" "pri ag0 trC" "pri ag0 trD" "pri ag0 trE" "pri ag0 trF" "pri ag1 tr0" "pri ag1 tr1" "pri ag1 tr2" "pri ag1 tr3" "pri ag1 tr4" "pri ag1 tr5" "pri ag1 tr6" "pri ag1 tr7" "pri ag1 tr8" "pri ag1 tr9" "pri ag1 trA" "pri ag1 trB" "pri ag1 trC" "pri ag1 trD" "pri ag1 trE" "pri ag1 trF"	1000000 1 00000 1000001 1 00000 1000010 1 00000 1000011 1 00000 1000100 1 00000 1000101 1 00000 1000110 1 00000 1000111 1 00000 1001000 1 00000 1001001 1 00000 1001010 1 00000 1001011 1 00000 1001100 1 00000 1001101 1 00000 1001110 1 00000 1001111 1 00000 1010000 1 00000 1010001 1 00000 1010010 1 00000 1010011 1 00000 1010100 1 00000 1010101 1 00000 1010110 1 00000 1010111 1 00000 1011000 1 00000 1011001 1 00000 1011010 1 00000 1011011 1 00000 1011100 1 00000 1011101 1 00000 1011110 1 00000 1011111 1 00000

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
RplyID = A23#, A21:16#, ADS#, REQ4:0# (13 bits) (continued)	"pri ag2 tr0" "pri ag2 tr1" "pri ag2 tr2" "pri ag2 tr3" "pri ag2 tr4" "pri ag2 tr5" "pri ag2 tr6" "pri ag2 tr7" "pri ag2 tr8" "pri ag2 tr9" "pri ag2 trA" "pri ag2 trB" "pri ag2 trC" "pri ag2 trD" "pri ag2 trE" "pri ag2 trF" "pri ag3 tr0" "pri ag3 tr1" "pri ag3 tr2" "pri ag3 tr3" "pri ag3 tr4" "pri ag3 tr5" "pri ag3 tr6" "pri ag3 tr7" "pri ag3 tr8" "pri ag3 tr9" "pri ag3 trA" "pri ag3 trB" "pri ag3 trC" "pri ag3 trD" "pri ag3 trE" "pri ag3 trF" " --- "	1100000 1 00000 1100001 1 00000 1100010 1 00000 1100011 1 00000 1100100 1 00000 1100101 1 00000 1100110 1 00000 1100111 1 00000 1101000 1 00000 1101001 1 00000 1101010 1 00000 1101011 1 00000 1101100 1 00000 1101101 1 00000 1101110 1 00000 1101111 1 00000 1110000 1 00000 1110001 1 00000 1110010 1 00000 1110011 1 00000 1110100 1 00000 1110101 1 00000 1110110 1 00000 1110111 1 00000 1111000 1 00000 1111001 1 00000 1111010 1 00000 1111011 1 00000 1111100 1 00000 1111101 1 00000 1111110 1 00000 1111111 1 00000 xxxxxxx x xxxxx

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
BE# = A15:8#, bqual#	"64/b7:0" "56/b6:0" "56/b7:0" "48/b5:0" "48/b7:1" "40/b4:0" "40/b7:2" "32/b3:0" "32/b4:1" "32/b5:2" "32/b6:3" "32/b7:4" "24/b2:0" "24/b7:5" "16/b1:0" "16/b2:1" "16/b3:2" "16/b4:3" "16/b5:4" "16/b6:5" "16/b7:6" " 8/b0 " " 8/b1 " " 8/b2 " " 8/b3 " " 8/b4 " " 8/b5 " " 8/b6 " " 8/b7 " "None " " --- "	0000 0000 0 1000 0000 0 0000 0001 0 1100 0000 0 0000 0011 0 1110 0000 0 0000 0111 0 1111 0000 0 1110 0001 0 1100 0011 0 1000 0111 0 0000 1111 0 1111 1000 0 0001 1111 0 1111 1100 0 1111 1001 0 1111 0011 0 1110 0111 0 1100 1111 0 1001 1111 0 0011 1111 0 1111 1110 0 1111 1101 0 1111 1011 0 1111 0111 0 1110 1111 0 1101 1111 0 1011 1111 0 0111 1111 0 1111 1111 0 xxxx xxxx x
SMMEM# = A7#, bqual	"Sys Mgt Mode Mem" " --- "	00 xx
SPLCK# = A6#, bqual#	"Split Lock" " --- "	00 xx
DEN# = A4#, bqual#	"Defer Enbl" " --- "	00 xx

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
RS#	" --- " "Retry " "Deferred " "RESERVED " "Hard Failure" "No Data " "Impl Wrtback" "Normal Data "	111 110 101 100 011 010 001 000
TRDY#	"Target Ready" " --- "	0 1
DRDY#	"Data Ready" " --- "	0 1
DBSY#	"Data Bus Busy" " --- "	0 1
AERR#	"Addr Par Error" " --- "	0 1
Error	"Addr Par Error" " --- "	11 x0
BERR#	"Bus Error" " --- "	0 1
BINIT#	"Bus Init" " --- "	0 1
RESET#	"Reset" " --- "	0 1
NMI	"Nonmask Intr Req" " --- "	1 0
INTR	"Interrupt" " --- "	1 0
FLUSH#	"Flush" " --- "	0 1
INIT#	"Init" "--- "	0 1
PREQ#	"Stopped" "Running"	0 1

Table 4. Pentium® Pro Symbols (Cont.)

Signal	Symbol	Value
PRDY#	"Probe Mode" " --- "	0 1
SMI#	"Sys Pow Mng Intr" " --- "	0 1
A20M#	"Addr 20 Mask" " --- "	0 1
STPCK#	"Stopped Clock" " --- "	0 1
IERR#	"Internal Error" " --- "	0 1
FRCERR	"Checker" "Master "	0 1
FERR#	"FP Error" " --- "	0 1
IGNNE#	"Ignore Num Excep" " --- "	0 1
bqual#	"Request B" " --- "	0 1
equal#	"Error" " --- "	0 1
squal#	"Snoop" " --- "	0 1
cqual#	"Trans Active" " --- "	0 1

To display captured state (transaction) data

Transaction tracking is available with the 16500B Logic System. For inverse assembly, the 16505A Prototype Analyzer is also required.

- **Select the Listing Menu for your logic analyzer.**

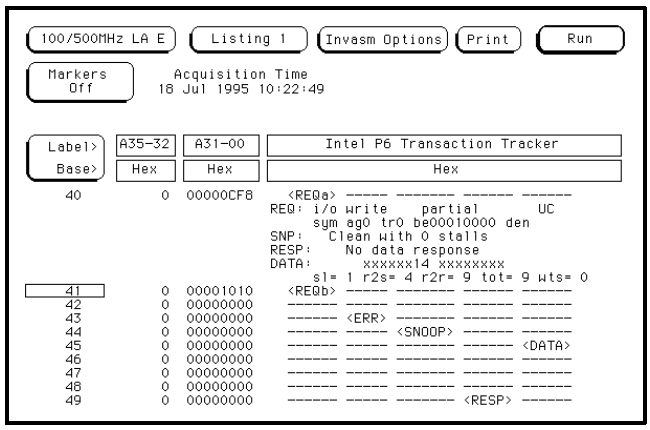
  The logic analyzer displays captured data in the Listing Menu. The transaction tracker processes the captured data in a transaction-based format.

  If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the preprocessor interface hardware is configured for state analysis. The "Invasm Options" field will appear at the top of the Listing Menu screen when the logic analyzer is configured for state analysis. See Chapter 1 to review the hardware configuration, correct it if needed, and then run the trace again.

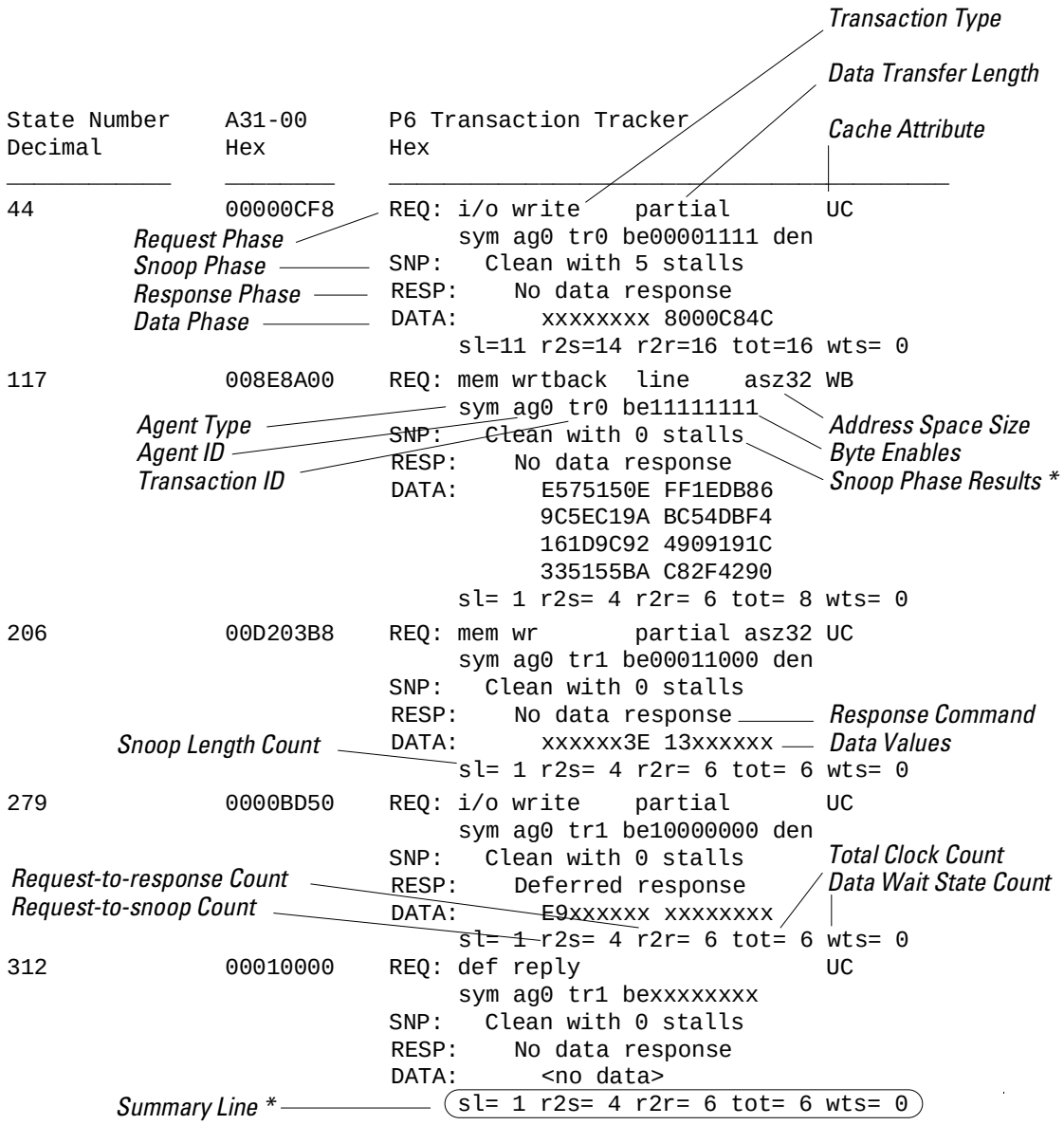
Example

Figure 7 shows the Listing Menu display for the 16550A logic analyzer using the IAP6B2E transaction tracker with the QUAL switch set for Expanded clock qualifier. Figure 8 shows the Listing Menu display with the QUAL switch set for Compacted clock qualifier (refer to "Modes of Operation" in chapter 3 for information on clock qualifiers). The listing on the following page highlights the various transactions captured by transaction tracker.

Figure 7

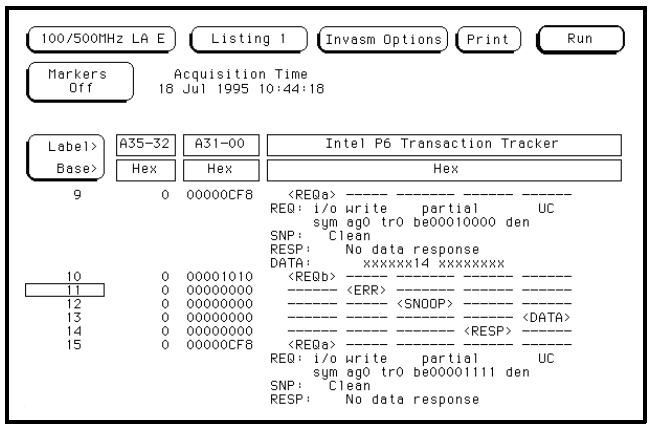


Logic Analyzer Listing Menu (Expanded Clock Qualifier)



* The Summary Line and Snoop Phase Stall Results are only displayed in the Listing Menu when using the Expanded clock qualifier.

Figure 8



Logic Analyzer Listing Menu (Compacted Clock Qualifier)

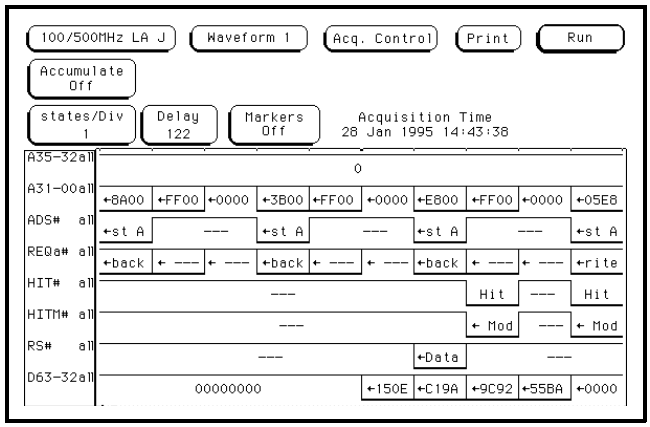
To display captured timing data

- Display the Waveform Menu for your logic analyzer.

Example

The following figure shows the Waveform Menu display for the Agilent Technologies 16550A logic analyzer:

Figure 9



Logic Analyzer Waveform Menu

This section discusses the general output format of the transaction tracker, and any processor-specific information you will need.

The transaction tracker supports many filter options based on type of states (start of a transaction, part of some transaction), transaction types, and transaction-agent ownership. The next few paragraphs describe the general output format of the transaction tracker.

Numeric Format

For the data phase (DATA:) display, the numeric output from the transaction tracker is in hexadecimal format. All other numbers are in decimal format.

Transaction Types

The Transaction Tracker displays the following Pentium® Pro information (when appropriate), fully correlated for each transaction.

Request Phase
- Address
- Transaction Type
  - Deferred Reply
  - Interrupt Acknowledge
  - Special Transactions
  - Branch Trace Message
  - I/O Read
  - I/O Write
  - Memory Read & Invalidate
  - Memory Read - Data
  - Memory Read - Code
  - Memory Write
  - Memory Writeback
- Address Size (32/36 or 32 bits)
- Transfer Length (partial or line)
- Cache Attribute (UC, USWC, WT, WP, WB)
- Agent Type (symmetric or priority)
- Agent ID
- Deferred Transaction ID
- Byte Enables
- Extended Functions
  - System Management Memory
  - Split Lock
  - Deferred Transaction Enable

Snoop Phase

Clean	Hit Modified
Hit	Deferred

Error Phase

Address Parity Termination (when observation policy enabled)

Response Phase

Response Command

Idle	Deferred
Retry	Hard Failure
No Data	Implicit Writeback
Normal Data	

Data Phase

Data Values (for appropriate bytes and chunks)

Summary Information (Expanded clock qualifier only)

Snoop Phase length (sl) in number of clocks (including all stalls)
Request-to-Snoop time (r2s) in number of clocks
Request-to-Response time (r2r) in number of clocks
Total transaction time (tot) in number of clocks
Total number of data wait states (wts) in number of clocks

Filter Options

The transaction tracker supports many filter options based on types of states (start of a transaction, part of some transaction), transaction types, and transaction ownership. The following is a list of the filter options available.

Filterable State	**Options**	**Associated Signals**
Non-request Phase A:	Show/Suppress	ADS#
Agents		ADS#, DID[7:0]# (Ab[23:16]#)
Symmetric 1:	Show/Suppress	
Symmetric 2:	Show/Suppress	
Symmetric 3:	Show/Suppress	
Symmetric 4:	Show/Suppress	
Priority:	Show/Suppress	

Filterable State	**Options**	**Associated Signals**
Transaction Types:		ADS#, REQa[4:0]#, REQb[4:0]#
Deferred Replies:	Show/Suppress	
Interrupt Acknowledge:	Show/Suppress	
Special Transactions:	Show/Suppress	
Branch Trace Msgs:	Show/Suppress	
I/O Reads:	Show/Suppress	
I/O Writes:	Show/Suppress	
Memory Read & Inv:	Show/Suppress	
Memory Reads - Data:	Show/Suppress	
Memory Reads - Code:	Show/Suppress	
Memory Writes:	Show/Suppress	
Memory Writebacks:	Show/Suppress	

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The preceding section shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function gives you a better analysis display in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Transaction Tracker Messages

Any of the following messages may appear during analysis of your target software. Included with each message is a brief explanation.

Errors and warnings

The Agilent Technologies E2466B software contains error messages and warnings for both the transaction tracker and the inverse assembler. For a list and description of the messages, refer to Appendix A.

Reserved status decodings

transaction types
- "RSVD (ignr)" -- Reserved (Ignore)
- "RSVD (CAR) " -- Reserved (Central Agent Response)
- "RSVD (MmWr)" -- Reserved (Memory Write)

data transfer length
- "RSVD" -- LEN = 01 -- 16 bytes -- not in P6.0DX
- "RSVD" -- LEN = 11 -- reserved address size
- "aszRS " - ASZ = 10
- "aszRS " - ASZ = 11

memory type
- "RSVD" -- ATTR2:0 = 001
- "RSVD" -- ATTR2:0 = 010
- "RSVD" -- ATTR2:0 = 011

reserved special transactions
- "special rsvd"

reserved response commands
- "Idle state *** ERROR ***" -- RS# = 111
- "RESERVED response " -- RS# = 100

Reaching boundaries

If the transaction tracker internal search limit (2000 states per transaction) is exceeded, or if part of a transaction is not acquired at the end of the analyzer acquisition memory, some or all of the following error messages may be displayed.

Snoop completion
"??? with >2000 stalls"

Response command
"unknown"

Data phase
"******** ********"

Summary line display
"sl=2000" "r2s=2000"
"r2r=2000" "tot=2000"
"wts=2000"

Protocol Violations

The transaction tracker displays a few Pentium Pro bus protocol violations. These are listed as follows:

rcnt = 0 or >8 during Request Phase B
scnt = 0 or >8 during Request Phase B
DRDY# or DBSY# not asserted during an incomplete data phase

Protocol violations are followed with line:
"*** protocol violation detected ***"

Note 4

The transaction tracker does not attempt to do a complete job of detecting protocol violations. Undetected protocol violations may cause the transaction tracker to display incorrect results.

Using the Inverse Assembler

In addition to basic transaction tracking, the Agilent Technologies 16505A can display an accurate instruction execution trace of Pentium® Pro target systems containing up to four processors. This feature is available only to users of the Agilent Technologies 16505A Prototype Analyzer. Instruction disassembly requires the use of a separate run-control tool to disable all CPU caches and enable Branch Trace Message transactions.

Operating modes are determined by a combination of preprocessor interface hardware switch settings and options selected in the Agilent Technologies 16505A Listing window under the "Invasm - Filter..." and "Invasm - Preferences..." menu pull-downs. The Filter dialog allows the user to show, suppress, or change the color of an entire acquisition state, whereas the Preferences dialog controls the display format for a state which is shown.

Hardware switches

The inverse assembler software requires that switches on the preprocessor interface hardware be set to one of the modes listed below.

- State Mode with Expanded Clock Qualifier
- State Mode with Compacted Clock Qualifier

Refer to the figure on page 1-5 for correct switch positions. If the switches are mistakenly set to Timing mode, the "inverse assembly" column in the Listing window displays the message

"<error: h/w in timing mode or clk qual off>".

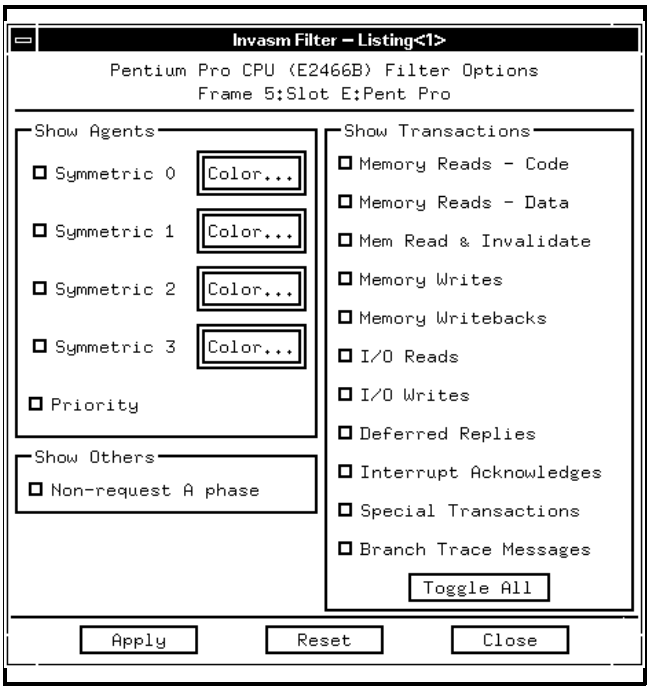
See Appendix A for a complete list of error messages.

Pentium® Pro filter dialog

The Filter dialog provides the ability to display only information for particular bus agents and/or transaction types. For multiprocessing target systems, a unique color can be used to identify transactions from each processor (symmetric agent). The figure below shows a sample Filter dialog.

Instruction disassembly is only possible when Branch Trace Messages are selected to be "shown" via the Filter dialog, are enabled for the target system, and instruction caches have been disabled.

Figure 10



Agilent Technologies 16505A Pentium® Pro Filter Dialog

Pentium® Pro preferences dialog

The Preferences dialog controls the level of detail for states shown.

Disassembly

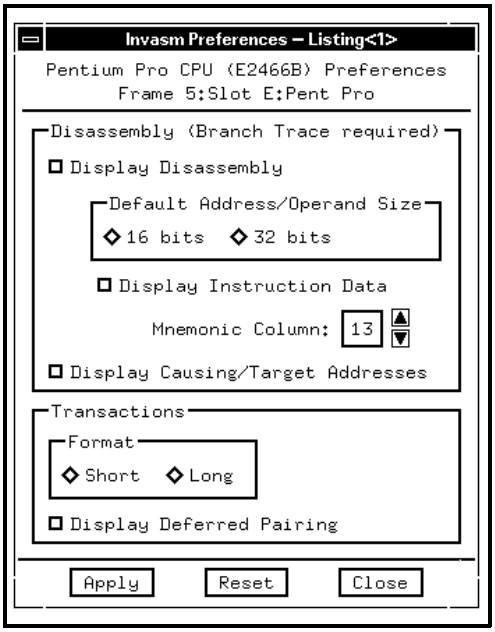
When Display Disassembly is selected, a block of instructions appears in the Listing window under each Branch Trace Message transaction or Memory Code Read from the reset vector (the instruction cache(s) must be disabled). The Default Address/Operand Size must be set appropriately for correct disassembly. If the last instruction in the block is non-branching, then the default size is most likely wrong or the instruction cache(s) have not been disabled. Display Instruction Data turns on/off the display of data bytes corresponding to each instruction. Display Causing/Target Addresses shows the causing and target linear addresses contained in each Branch Trace Message transaction.

Transactions

The transaction Format can be set to Short to display one line per transaction data chunk (DRDY# asserted state), or Long for more extensive information about the request, snoop, and response phases. Display Deferred Pairing consolidates the deferred reply transaction information directly beneath the original deferred transaction.

Disassembly is only possible when Display Disassembly is selected in the Preferences dialog and Branch Trace Messages are selected in the Filter dialog. Additionally, a run-control tool should be used to enable Branch Trace Messages and disable the instruction caches for all processors.

Figure 11



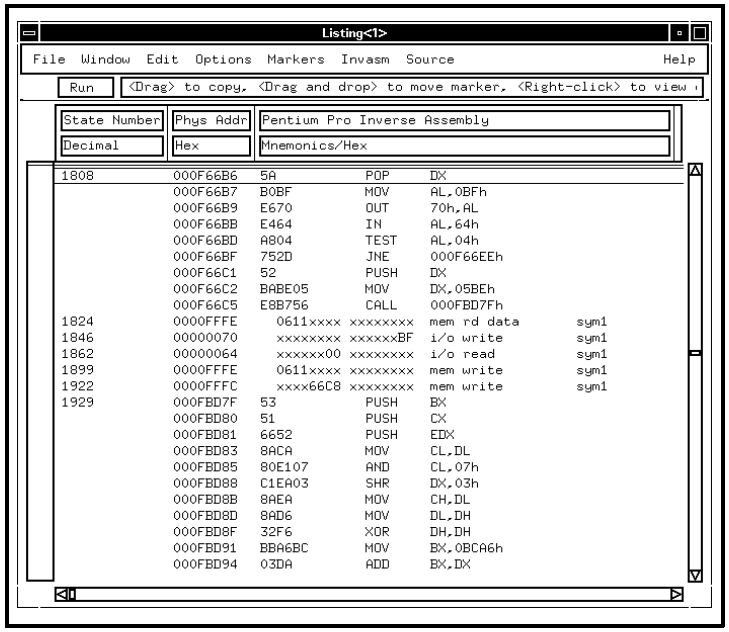
Agilent Technologies 16505A Pentium® Pro Preferences Dialog

Suggested Settings

For software analysis, the settings below give a high-level view of the captured data. Remember to disable the processor instruction caches and enable Branch Trace Messages in order to get disassembly.

Switches:	State Mode with Compacted Clock Qualifier.	
Filter:	Show Agents	-- Show All
	Show Transactions	-- Show All except Memory Reads-Code
	Show Others	-- Suppress Non-Request A Phases
Preferences:	Display Disassembly	-- ON
	Display Causing/Target Addresses	-- OFF
	Transaction Format	-- SHORT
	Display Deferred Pairing	-- ON

Figure 12



Agilent Technologies 16505A Listing window for Software Analysis

For hardware analysis, the settings below provide detailed phase information on each transaction.

Switches:	State Mode with Expanded Clock Qualifier.	
Filter:	Show Agents	-- Show All
	Show Transactions	-- Show All
	Show Others	-- Show All
Preferences:	Display Disassembly	-- OFF
	Display Causing/Target Addresses	-- ON
	Transaction Format	-- LONG
	Display Deferred Pairing	-- OFF

Disassembler Behavior

To display instruction disassembly, use a Pentium® Pro run-control tool to enable Branch Trace Messages and disable the processor instruction caches. In the Filter dialog, show Branch Trace Messages, and select Display Disassembly in the Preferences dialog.

When a processor executes a branching instruction, the prefetch queues are flushed, a Branch Trace Message (BTM) appears on the bus, and the processor begins fetching code at the branch target address. The disassembly software finds matching code reads between the current BTM and the next matching BTM, reorders any out-of-order bursts, then disassembles the code read data. In searching for code reads, any fetches which are deferred are automatically paired with their corresponding deferred replies to ensure that all code read data is found. This pairing is not affected by the Display Deferred Pairing setting in the Preferences dialog.

In a block of disassembled instructions for a Branch Trace Message, the last instruction must cause a branch (by definition). If the last instruction is displayed as non-branching and the next BTM is present, then CPU instruction caches are not disabled or the Default Address/Operand Size setting is incorrect. Open the "Invasm - Preferences..." dialog, change the default size, and click on Apply. If the problem persists, then the data may be corrupt. Verify that the logic analyzer cables are properly connected for D[63-32] and D[31-00].

Physical vs. Linear Addresses

Branch Trace Messages give linear causing and target addresses. The addresses displayed for Memory Code Read transactions are physical. For real-mode programs, this is not an issue since linear and physical addresses are equivalent. For protected-mode programs with paging enabled, the

address bits higher than A[11] will usually be different. Physical addresses for disassembled instructions are shown in the "Phys Addr" column of the Listing window to make it easier to trigger upon or find in the Listing which Memory Code Read transaction resulted in a particular instruction.

Special Case

If the next Branch Trace Message is missing but the first code read is found, the software disassembles all matching code reads up to the point where the search terminated at a reset, bus initialization, end of acquisition, or search-limit-exceeded state. Disassembly accuracy is not guaranteed in this case.

The following table describes the reset configuration information that is displayed at reset.

Table 5. Reset Configuration

Signal at Reset	Configuration (asserted/deasserted)
FLUSH#	Output Tristate Enabled/Disabled
INIT#	Built-in Self Test Enabled/Disabled
A8#	AERR# Observation Policy Enabled/Disabled
A9#	BERR# Observation Policy Enabled/Disabled
A10#	BINIT# Observation Policy Enabled/Disabled
A7#	In-order Queue depth = 1/8
A6#	Power-on Reset Vector = 000FFFF0 or FFFFFFF0 hex
A5#	FRC Mode Enabled/Disabled
A[12:11]#	APIC Cluster ID (00, 01, 10, 11)

Triggering Hints

Storage Qualification

Any use of storage qualification in the trigger sequence will result in error messages in the inverse assembly column in the Listing. The preprocessor interface communicates its switch settings and dynamic AERR/BINIT observation policies to the logic analyzer via a repeating serial frame on the preprocessor-generated "config" signal. Storage qualification interrupts this serial frame, resulting in transaction tracker/disassembler errors.

Triggering on address errors

To trigger on an address error, use the Error label symbol. The Error label combines the AERR# signal with the equal# error phase signal. Set up the trigger menu sequencer level to "while storing anystate, trigger on a", where a = "Addr Par Error" (Error label in symbol base).

Triggering on data and transaction type

There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Although the Listing displays a transaction type and 8-byte data value on the same line when Transaction Display Mode is set to Short, this alignment is the result of post-processing and cannot be used for triggering. The preprocessor interface hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type in the Request A phase, then trigger on a data value qualified by DRDY# asserted; however, by the time the data pattern is found, it could belong to a different transaction.

Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and REQa# labels, together with the REQa# label. The REQa# label consists of the REQ[4:0]# signals and the ADS# signal. Its symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

Triggering on address, transaction type, and Request Phase B information

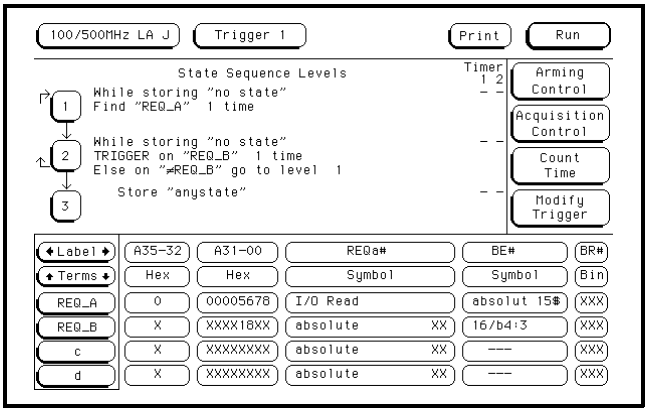
To trigger on a specific address, transaction type and Request Phase B information, follow the instructions given in the previous paragraph, and then set up a second sequence level which includes the label(s) for the Request Phase B information that you are interested in, such as DID#, BE#, ATTR#, etc. Labels such as DID#, BE#, and ATTR# contain the Request Phase B qualifier, so triggering on valid Request Phase B states is assured.

Set up a loop from the 2nd sequence level such that the sequencer will return to level 1 if the Request Phase B condition is not found.

Example

In this example, the sequencer is set to trigger on a 16-bit I/O Read at address 00000567A hex. The 2nd sequence level will return to level 1 if the Request Phase B condition is not found

Figure 13



Logic Analyzer State Sequence Levels for Triggering

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the Agilent Technologies E2466B hardware including the characteristics and signal mapping for the preprocessor interface. This chapter also includes a brief theory of operation, circuit board dimensions, and information on servicing the preprocessor interface.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Table 6. Operating Characteristics

Microprocessor Compatibility	Intel Pentium® Pro microprocessor	
Microprocessor Package	387-pin staggered PGA	
Clock Frequency	66 MHz maximum for external BCLK	
Target Signal Amplitude	800 mV p-p minimum for all GTL+ signals	
Logic Analyzers Supported	16550A (two card) 16554A (three card) 16555A (three card) 16556A (three card)	
Accessories Required	None.	
Timing Analysis	3 nS channel-to-channel skew (typical)	
Power Requirements	Supplied by the logic analyzer.	
Probes Required	Ten logic analyzer pods are required for transaction tracking.	
Signal Line Loading	Varies (see description on following page).	
Environmental Temperature	Operating Nonoperating	0 to 55 degrees C (+32 to +131 degrees F) -40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating Nonoperating	4,600 m (15,000 ft) 15,300 m (50,000 ft)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Signal line loading

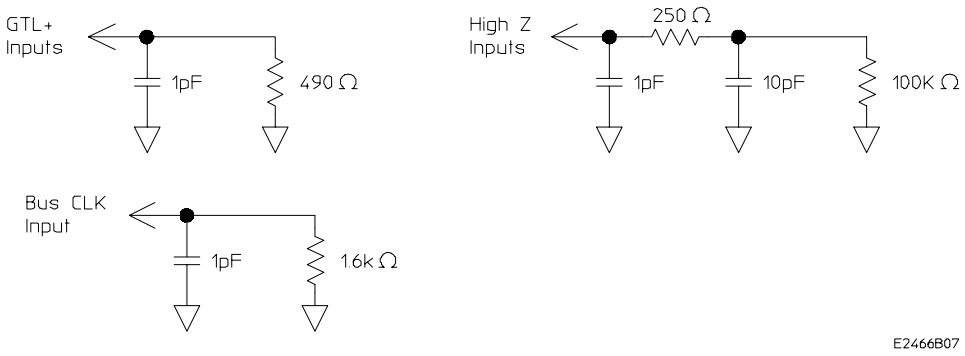
The figure below shows the equivalent loads placed on the microprocessor bus by the preprocessor interface. The loading is not affected by the preprocessor operating mode.

The high-impedance model applies to the following list of signals:

Table 7. High Z Inputs

3.3V Tolerant	APIC Group	JTAG Group
A20M#	PICCLK	TCLK
FERR#	PICD1#	TRST#
FLUSH#	PICD0#	TMS
IERR#		TDI
IGNNE#		TDO
INIT#		
LINT0/INTR		
LINT1/NMI		
PREQ#		
SMI#		
STPCLK#		

Figure 14



Signal Line Loading

Modes of operation

The preprocessor interface can operate in State mode or Timing mode. In State mode, the logic analyzer master clock is always qualified with the "cqual#" signal from the preprocessor. This clock qualifier is set to either Compacted or Expanded. By eliminating idle clocks, the Compacted qualifier can potentially capture many more transactions than the Expanded qualifier. Refer to chapter 1 for information on configuring the preprocessor interface and logic analyzer for the desired mode of operation.

State Mode Operation

State mode uses the Pentium® Pro BCLK rising edge to capture the signals from the Pentium® Pro bus and to clock the logic analyzer. A PLD in the preprocessor generates additional information about each Pentium Pro clock. The PLD information along with the Pentium® Pro signals are sent to the logic analyzer and used by the transaction tracker and inverse assembler to produce the Pentium® Pro transaction display (see figure 15, Block Diagram).

Pentium® Pro signals require a three-clock latency to move the Pentium® Pro information from the Pentium® Pro pins to the logic analyzer memory (except for the three Pentium® Pro signals on connector P1, which only require two clocks). The first clock is used to capture all of the Pentium® Pro signals in latches on the preprocessor. The second clock is used to move the Pentium® Pro signals from the preprocessor latches into the logic analyzer slave register. The slave latches exists within the logic analyzer, not in the preprocessor. Also, on the second clock, the PLD uses the Pentium® Pro signals that were captured on the first clock to generate additional information (see below). The third clock is used by the logic analyzer to trigger on and/or store the Pentium® Pro data and the PLD information.

Preprocessor generated signals

The PLD on the preprocessor generates the following signals when operated in State mode:

Request Count - rcnt[3:0] The request count is the number of transactions outstanding on the bus. It is incremented whenever ADS# is asserted, and decremented when a response is asserted. It is also decremented when a transaction is terminated in the error phase. It is used by the transaction tracking software to reconstruct transactions.

Snoop Count - scnt[3:0] The snoop count is a running count of the number of pending transactions that have not completed their snoop phases. It is incremented whenever ADS# is asserted, and decremented when a snoop phase completes. It is also decremented when a transaction is terminated in the error phase. It is used by the transaction tracking software to reconstruct transactions.

Request Phase B Qualifier - bqual# The Request Phase B qualifier is asserted during the clock after a Request Phase A has taken place. It effectively is the ADS# signal delayed by one clock. It is used in Request phase B signal label symbols, so that these symbols are only displayed during request phase B states.

Error Phase Qualifier - equal# The error phase qualifier is always asserted during the error phase of a transaction. It is unaffected by the AERR# observation policy or whether the AERR# signal is asserted.

Snoop Phase Qualifier - squal# In State mode with the Expanded clock qualifier, this signal is asserted on the "odd" clocks of the snoop phase. The "odd" clocks are those in which the HIT# and HITM# signals are observed. The snoop qualifier is not asserted during the "even" clocks which occur between snoop stall clocks.
In State mode with the Compacted clock qualifier, this signal is asserted only on the last clock of a snoop phase (NOT asserted for snoop stalls).

Clock Qualifier - cqual# In State mode with the Expanded clock qualifier, this signal is asserted while any transactions are outstanding, while RESET# is asserted, and for the first clock after RESET# is deasserted.
In State mode with the Compacted clock qualifier, this signal is asserted for the following conditions:

Request A and B phases
Error phase
Snoop phase (last clock only)
Response phase
Data phase (when DRDY# is asserted)
first clock after a rising/falling transition occurs on RESET#
first clock when TRDY# is seen asserted with DBSY# deasserted
first clock after TRDY# is deasserted

Pentium® Pro signals are unconditionally clocked into the logic analyzer slave latches. On the next clock, if the clock qualifier is asserted at the slave latch input, then the slave latches contents are stored into memory along

with the previous clock qualifier value. Therefore, although "cqual#" can be displayed in the listing and waveform menus, its value is meaningless.

State Mode Clocking

To utilize the logic analyzer slave latches, the logic analyzer is configured to operate in "master/slave" mode. The logic analyzer uses the Pentium® Pro BCLK [L↑] to capture all pod data, except the pod connected to preprocessor connector P1, in the slave register. Connector P1 carries the PLD signals and is assigned to the master clock [(L↑) • (M = 0)] which clocks the PLD information and the slave register outputs into the logic analyzer. The "cqual#" (M = 0) signal from the PLD is used to qualify the master clock to eliminate the collection of unnecessary Pentium® Pro data.

> The logic analyzer master clock must always include the M=0 qualifier for the transaction tracker to operate properly.

State Mode Buffered Signals

In state mode, most of the Pentium® Pro signals are latched by the bus clock before being routed to the logic analyzer. The following signals, however, are always buffered instead of latched:

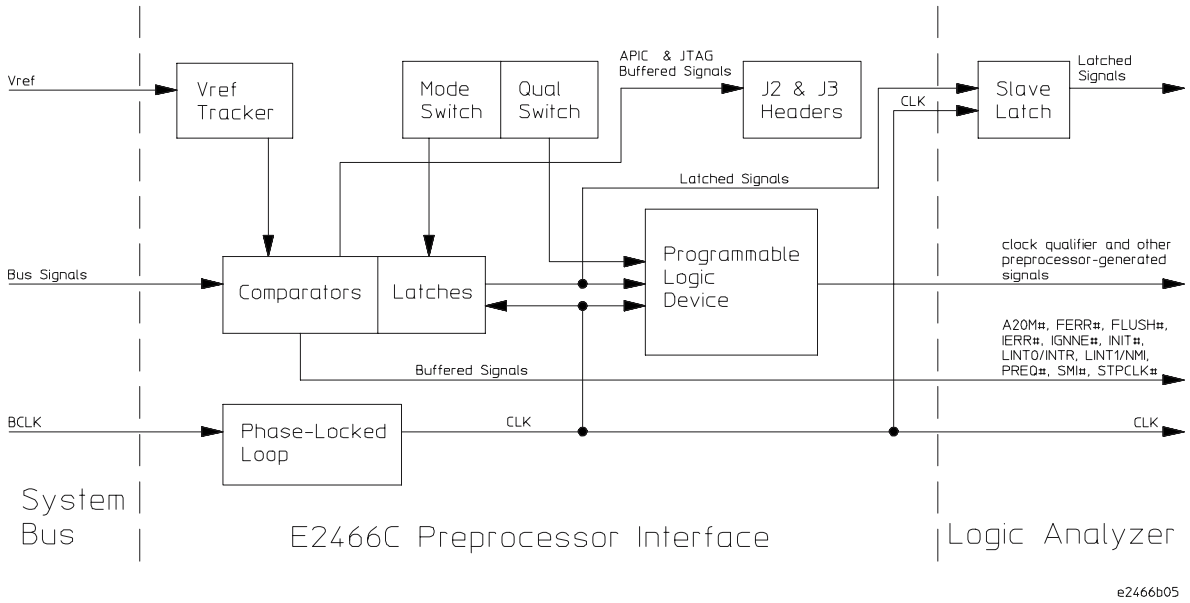
APIC & JTAG groups
A20M#
FERR#
FLUSH#
IERR#
IGNNE#
INIT#
LINT0/INTR
LINT1/NMI
PREQ#
SMI#
STPCLK#

Timing Mode Operation

The E2466B acts as a buffer in timing mode. The buffer in the preprocessor passes each Pentium® Pro signal to the logic analyzer regardless of the state of BCLK. The slave latch within the logic analyzer is also bypassed and the PLD does not generate supplemental information. The transaction tracker will not operate when the preprocessor is in timing mode.

Agilent Technologies E2466B Block Diagram

Figure 15



Agilent Technologies E2466B Block Diagram

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the Agilent Technologies E2466B Preprocessor Interface. Since the pods on the
logic analyzers are numbered differently than the preprocessor connectors, refer to the tables in chapter 1 to correlate the pod numbers.

The signal list table column descriptions are as follows:

PREPROCESSOR CONNECTOR	NAME	The preprocessor connector that carries the signal.
	PIN	The pin within the preprocessor connector that carries the signal.
	BIT	The bit position of the signal within the preprocessor connector.
CPU	SIGNAL	The microprocessor signal name.
	PIN #	The processor pin number for the signal.
ANALYZER	LABEL(S)	The analyzer label assigned to the signal. Lower case letters indicate a preprocessor generated signal.

Table 8. Pentium® Pro Signal List

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P1	3	CLK1	BCLK	A19	BCLK
P1	7	D15	LINT0/INTR	AG43	LINT0 **
P1	9	D14	FLUSH#	A15	FLUSH# **
P1	11	D13	INIT#	C11	INIT# **
P1	13	D12		*	squal#
P1	15	D11		*	bqual#
P1	17	D10		*	rcnt
P1	19	D9		*	rcnt
P1	21	D8		*	rcnt
P1	23	D7		*	rcnt
P1	25	D6		*	scnt
P1	27	D5		*	scnt
P1	29	D4		*	scnt
P1	31	D3		*	scnt
P1	33	D2		*	equal#
P1	35	D1		*	mqual#
P1	37	D0		*	config

* These signals are generated by the preprocessor interface.
** These signals are buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P2	3	CLK1		*	cqual#
P2	7	D15	BR3#	U9	BR#
P2	9	D14	BR2#	AA1	BR#
P2	11	D13	BR1#	W3	BR#
P2	13	D12	BR0#	AC5	BR#
P2	15	D11	BPRI#	U5	BPRI#
P2	17	D10	BNR#	U7	BNR#
P2	19	D9	LOCK#	AA9	LOCK#
P2	21	D8	ADS#	AE3	ADS#
P2	23	D7	REQ4#	W5	REQ#
P2	25	D6	REQ3#	Y1	REQ#
P2	27	D5	REQ2#	Y3	REQ#
P2	29	D4	REQ1#	W7	REQ#
P2	31	D3	REQ0#	W9	REQ#
P2	33	D2	HIT#	AC3	HIT#
P2	35	D1	HITM#	AA7	HITM#
P2	37	D0	DEFER#	Y5	DEFER#

* These signals are generated by the preprocessor interface.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P3	3	CLK1	IGNNE#	A9	IGNNE# **
P3	7	D15	D15#	C37	D31-00
P3	9	D14	D14#	A37	D31-00
P3	11	D13	D13#	A43	D31-00
P3	13	D12	D12#	C35	D31-00
P3	15	D11	D11#	A41	D31-00
P3	17	D10	D10#	A39	D31-00
P3	19	D9	D9#	A35	D31-00
P3	21	D8	D8#	A33	D31-00
P3	23	D7	D7#	C33	D31-00
P3	25	D6	D6#	C31	D31-00
P3	27	D5	D5#	A31	D31-00
P3	29	D4	D4#	C29	D31-00
P3	31	D3	D3#	A29	D31-00
P3	33	D2	D2#	C27	D31-00
P3	35	D1	D1#	A27	D31-00
P3	37	D0	D0#	C25	D31-00

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P4	3	CLK1	FERR#	C17	FERR# **
P4	7	D15	D31#	G47	D31-00
P4	9	D14	D30#	G43	D31-00
P4	11	D13	D29#	G41	D31-00
P4	13	D12	D28#	G45	D31-00
P4	15	D11	D27#	G39	D31-00
P4	17	D10	D26#	E47	D31-00
P4	19	D9	D25#	E43	D31-00
P4	21	D8	D24#	E45	D31-00
P4	23	D7	D23#	E41	D31-00
P4	25	D6	D22#	E39	D31-00
P4	27	D5	D21#	C47	D31-00
P4	29	D4	D20#	C41	D31-00
P4	31	D3	D19#	C45	D31-00
P4	33	D2	D18#	C43	D31-00
P4	35	D1	D17#	C39	D31-00
P4	37	D0	D16#	A45	D31-00

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P5	3	CLK1	FRCERR	C9	FRCERR
P5	7	D15	D47#	N43	D63-32
P5	9	D14	D46#	Q47	D63-32
P5	11	D13	D45#	N41	D63-32
P5	13	D12	D44#	N39	D63-32
P5	15	D11	D43#	L43	D63-32
P5	17	D10	D42#	N45	D63-32
P5	19	D9	D41#	N47	D63-32
P5	21	D8	D40#	L41	D63-32
P5	23	D7	D39#	L47	D63-32
P5	25	D6	D38#	J43	D63-32
P5	27	D5	D37#	L39	D63-32
P5	29	D4	D36#	L45	D63-32
P5	31	D3	D35#	J41	D63-32
P5	33	D2	D34#	J47	D63-32
P5	35	D1	D33#	J45	D63-32
P5	37	D0	D32#	J39	D63-32

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P6	3	CLK1	IERR#	C3	IERR# **
P6	7	D15	D63#	W43	D63-32
P6	9	D14	D62#	Y47	D63-32
P6	11	D13	D61#	W45	D63-32
P6	13	D12	D60#	U43	D63-32
P6	15	D11	D59#	S39	D63-32
P6	17	D10	D58#	W47	D63-32
P6	19	D9	D57#	S41	D63-32
P6	21	D8	D56#	U45	D63-32
P6	23	D7	D55#	U47	D63-32
P6	25	D6	D54#	S43	D63-32
P6	27	D5	D53#	S45	D63-32
P6	29	D4	D52#	Q41	D63-32
P6	31	D3	D51#	Q39	D63-32
P6	33	D2	D50#	S47	D63-32
P6	35	D1	D49#	Q43	D63-32
P6	37	D0	D48#	Q45	D63-32

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P7	3	CLK1	STPCLK#	A3	STPCK# **
P7	7	D15	A15#, BE7#	L5	A31-00, BE#
P7	9	D14	A14#, BE6#	N3	A31-00, BE#
P7	11	D13	A13#, BE5#	N7	A31-00, BE#
P7	13	D12	A12#, BE4#	N1	A31-00, BE#
P7	15	D11	A11#, BE3#	N5	A31-00, BE#
P7	17	D10	A10#, BE2#	Q9	A31-00, BE#
P7	19	D9	A09#, BE1#	Q1	A31-00, BE#
P7	21	D8	A08#, BE0#	Q7	A31-00, BE#
P7	23	D7	A07#, EXF4#	Q3	A31-00, EXF#
P7	25	D6	A06#, EXF3#	S1	A31-00, EXF#
P7	27	D5	A05#, EXF2#	Q5	A31-00, EXF#
P7	29	D4	A04#, EXF1#	S3	A31-00, EXF#
P7	31	D3	A03#, EXF0#	S5	A31-00, EXF#
P7	33	D2	A02# tied high	--	A31-00
P7	35	D1	A01# tied high	--	A31-00
P7	37	D0	A00# tied high	--	A31-00

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P8	3	CLK1	A20M#	A11	A20M# **
P8	7	D15	A31#, ATTR7#	G9	A31-00, ATTR#
P8	9	D14	A30#, ATTR6#	E3	A31-00, ATTR#
P8	11	D13	A29#, ATTR5#	E1	A31-00, ATTR#
P8	13	D12	A28#, ATTR4#	J9	A31-00, ATTR#
P8	15	D11	A27#, ATTR3#	G5	A31-00, ATTR#
P8	17	D10	A26#, ATTR2#	G7	A31-00, ATTR#
P8	19	D9	A25#, ATTR1#	L9	A31-00, ATTR#
P8	21	D8	A24#, ATTR0#	G3	A31-00, ATTR#
P8	23	D7	A23#, DID7#	J7	A31-00, DID#
P8	25	D6	A22#, DID6#	G1	A31-00, DID#
P8	27	D5	A21#, DID5#	J3	A31-00, DID#
P8	29	D4	A20#, DID4#	J5	A31-00, DID#
P8	31	D3	A19#, DID3#	J1	A31-00, DID#
P8	33	D2	A18#, DID2#	L7	A31-00, DID#
P8	35	D1	A17#, DID1#	N9	A31-00, DID#
P8	37	D0	A16#, DID0#	L3	A31-00, DID#

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P9	3	CLK1	SMI#	W1	SMI# **
P9	7	D15	RSP#	U3	RSP#
P9	9	D14	RP#	AC7	RP#
P9	11	D13	DEP7#	U39	DEP#
P9	13	D12	DEP6#	Y45	DEP#
P9	15	D11	DEP5#	AA47	DEP#
P9	17	D10	DEP4#	W41	DEP#
P9	19	D9	DEP3#	AC47	DEP#
P9	21	D8	DEP2#	W39	DEP#
P9	23	D7	DEP1#	Y43	DEP#
P9	25	D6	DEP0#	AC45	DEP#
P9	27	D5	AP1#	S9	AP#
P9	29	D4	AP0#	U1	AP#
P9	31	D3	A35#	C1	A35-32
P9	33	D2	A34#	E9	A35-32
P9	35	D1	A33#	E7	A35-32
P9	37	D0	A32#	E5	A35-32

** This signal is buffered (not latched) in State mode.

Table 8. Pentium® Pro Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU		ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**PIN #**	**LABEL(S)**
P10	3	CLK1	LINT1/NMI	AG41	LINT1, NMI**
P10	7	D15	RS2#	AE7	RS#
P10	9	D14	RS1#	AE5	RS#
P10	11	D13	RS0#	AC9	RS#
P10	13	D12	TRDY#	Y9	TRDY#
P10	15	D11	DRDY#	AA3	DRDY#
P10	17	D10	DBSY#	AA5	DBSY#
P10	19	D9	AERR#	AE9	AERR#
P10	21	D8	BERR#	C5	BERR#
P10	23	D7	BINIT#	AC43	BINIT#
P10	25	D6	RESET#	Y41	RESET#
P10	27	D5	PREQ#	AA45	PREQ# **
P10	29	D4	PRDY#	Y39	PRDY#
P10	31	D3	BP3#	AC39	BP3#
P10	33	D2	BP2#	AE43	BP2#
P10	35	D1	BPM1#	AA39	BPM1#
P10	37	D0	BPM0#	AC41	BPM0#

** These signals are buffered (not latched) in State mode.

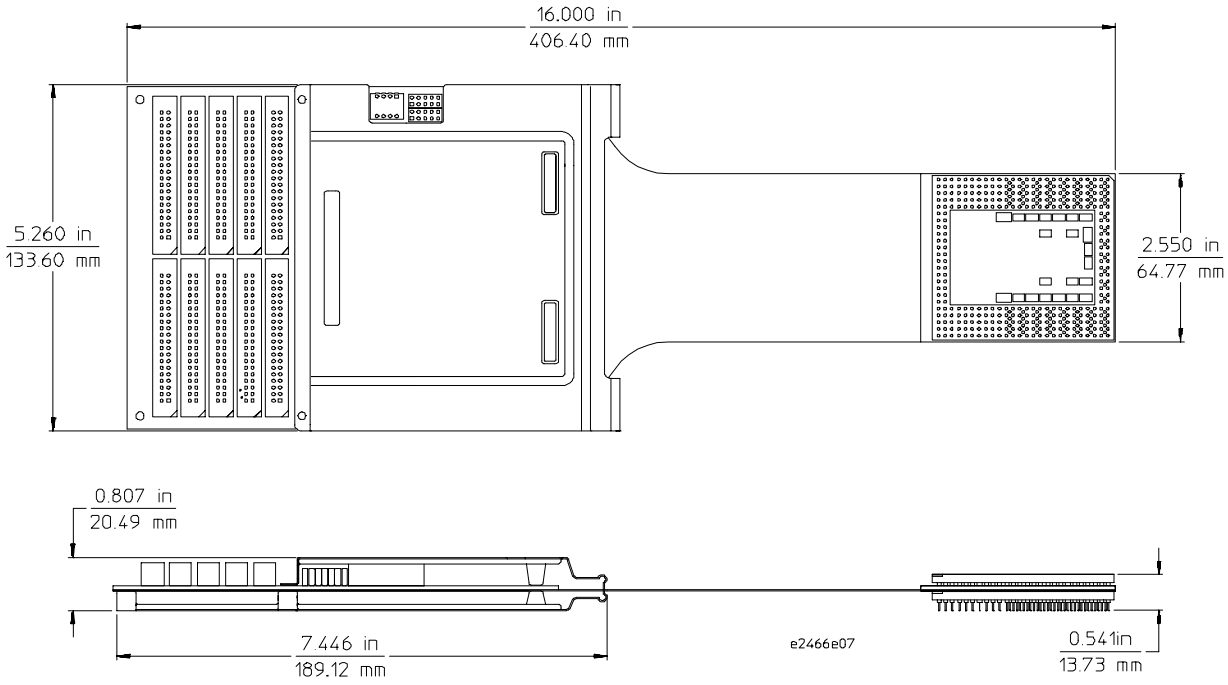
Table 8. Pentium® Pro Signal List (Cont.)

J2 (APIC)					J3 (JTAG)			
Pin #	**Signal**	**Signal**	**Pin #**		**Pin #**	**Signal**	**Signal**	**Pin #**
10	n/c	n/c	9		10	GND	TRST#	9
8	n/c	Ireset	7		8	GND	TDO	7
6	GND	PICD1#	5		6	GND	TDI	5
4	GND	PICD0#	3		4	GND	TMS	3
2	GND	PICCLK	1		2	GND	TCK	1
Refer to chapter 1 for additional information on connecting to these signals.								

Circuit Board Dimensions

The figure below gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.

Figure 16



Agilent Technologies E2466B Dimensions

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 9. Replaceable Parts

Agilent Part Number	Description
E2466-69506	Preprocessor Interface Circuit Board Exchange Assembly
E2466-68704	Software disk pouch
1200-1927	Pin Protector Socket

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reconnect all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Check that the logic analyzer threshhold is set for TTL levels.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor (if socketed) or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the preprocessor and target system.**

  1. **Power up the analyzer and preprocessor.**
  2. **Power up the target system.**

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.**

- ☐ **Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.**

- ☐ **Reduce the number of extender sockets.**

See Also "Capacitive Loading" in this appendix.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and transaction tracker failures.

- ☐ **Ensure that the preprocessor operating mode switches are correctly set for the measurement you are trying to make.**
- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.
- ☐ **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See “Capacitive Loading” in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.
- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz, or that have fast edge speeds.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

Transaction Tracker/Inverse Assembler Problems

This section lists problems that you might encounter while using the transaction tracker/inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and transaction tracker/inverse assembler correctly, you can proceed with confidence in debugging your target system.

No transaction tracking or incorrect transaction tracking

- ☐ **Ensure that each logic analyzer pod is connected to the correct preprocessor connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address, data, and status information to the analyzer in a predefined order. The cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the ADDR, ADDR_B, DATA, DATA_B, STAT, STAT_0, and STAT_1 format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. See Chapter 2 for more information.

- ☐ **Verify that storage qualification has not excluded storage of all the needed transaction phase information.**

Transaction tracker/inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the transaction tracker/inverse assembler is on the same disk as the configuration files you are loading and is in the same directory on the Agilent Technologies 16500B mainframe. For the Agilent Technologies 16505A Prototype Analyzer the transaction tracker must be in the /hp16505/ia directory.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding transaction tracker/inverse assembler for the Pentium® Pro. If you delete the transaction tracker/inverse assembler file or rename it, the configuration process will fail to load the transaction tracker/inverse assembler file properly.

  See Chapter 1 for details.

Transaction tracker/inverse assembler errors and warnings

********** ******** (no data displayed in the transaction display)**
It is common for transactions near the end of the acquisition to be clipped such that not all transactions phases are captured. In this case, any data states which are missing will be indicated by a row of asterisks.

<error: h/w in timing mode or clk qual off> The Agilent Technologies E2466B Preprocessor Interface hardware switches are not set to state mode, the master clock is not set to (L↑)*(M=0) in the Agilent Technologies 16505A Format window, or the logic analyzer cables are not connected properly to the preprocessor interface. Note that the clock qualifier must always be used, and storage qualification is not allowed in the trigger specification for proper transaction tracker/inverse assembler operation.

<error: sync lost (try resetting target)> The preprocessor interface hardware tracks the processor bus from reset. If the logic analyzer is turned off while the target is on, or if the preprocessor switches are

changed while the target is on, synchronization with the processor bus is lost. To correct this error, reset the target.

<error: BTM without CPU caches disabled> Because disassembly was selected in Preferences dialog, instructions would normally be displayed for the current Branch Trace Message transaction. If the next BTM was found, but the code read at the branch target address for the current BTM is missing, then this error results. To correct this error, disable all processor instruction caches.

<warning: too few states -- modes assumed> The preprocessor interface communicates its switch settings and dynamic AERR/BINIT observation policies to the logic analyzer via a repeating serial frame on the preprocessor-generated "config" signal. This error indicates that not enough states were acquired by the logic analyzer to contain a full serial frame. The software makes the assumptions listed below.

-- State Mode with Compacted Clock Qualifier

-- AERR/BINIT observation policies disabled

<warning: next BTM missing -- IA not guaranteed> Disassembled instructions are displayed as a continuous block for each Branch Trace Message (BTM) transaction. For any given BTM, the software searches for the next BTM to determine which instruction caused a branch to be taken. Near the end of acquisition, the next BTM may be incomplete or missing. Also, if the number of states to the next BTM exceeds the internal search limit, it will be treated as missing. Since the last instruction of the block is unknown, the software simply disassembles all memory code reads for a particular CPU from the current Branch Trace Message to the end of acquisition. Instructions may be displayed which were prefetched but never executed.

<warning: BTM without first code read> This warning indicates that the next Branch Trace Message was not found, and the code read at the branch target address for the current BTM was missing. Therefore no disassembled instructions are displayed for this state.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms another measurement module, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Logic Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the Pentium® Pro transaction tracker/inverse assembler that is attached to the configuration file. Ensure that the transaction tracker/inverse assembler file is not renamed or deleted.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for the Agilent Technologies 16550B cards. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.

See Also The *Agilent Technologies 16550B Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the Agilent Technologies 16500B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.**

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the Agilent Technologies 16500B or 16501A frame. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name: Agilent Technologies

Manufacturer's Address: Digital Design Product Generation Unit
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

declares, that the product

Product Name: Preprocessor

Model Number(s): Agilent Technologies E2466B

Product Option(s): All

conforms to the following Product Specifications:

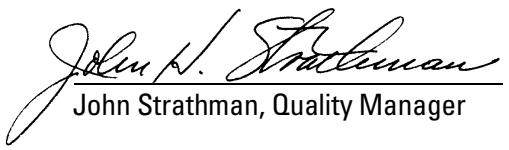
Safety:	IEC 348:1978 / HD 401 S1:1981	
	UL 1244	
	CSA-C22.2 No. 231 (Series M-89)	
EMC:	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 555-2:1982 + A1:1985 / EN 60555-2:1987	
	IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991	
	IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
	IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
	IEC 801-4:1988 / EN 50082-1:1992	0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

The Agilent Technologies 2466B preprocessor was tested with the Agilent Technologies 16500B mainframe and the Agilent Technologies 16550A plug-in logic analyzer.

Colorado Springs, 7/26/95



John Strathman, Quality Manager

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Product Regulations

Safety

IEC 348:1978 / HD 401 S1:1981
UL 1244
CSA-C22.2 No.231 (Series M-89)

EMC

CE
ISM 1-A

This Product meets the requirements of the European Communities (EC) EMC Directive 89/336/EEC.

Emissions EN55011/CISPR 11 (ISM, Group 1, Class A equipment)

Immunity

EN50082-1	Code[1]	Notes[2]
IEC 555-2	1	
IEC 555-3	1	
IEC 801-2 (ESD) 8 kV AD	2	1,2
IEC 801-3 (Rad.) 3 V/m	1	
IEC 801-4 (EFT) 1 kV	2	

[1] Performance Codes:
1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

[2] Notes:
1 The probe assembly is sensitive to ESD events. Use standard ESD preventive practices to avoid component damage.
2 Electrostatic discharges applied to the 16500B mainframe.

Sound Pressure Level N/A

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Safety Symbols

WARNING

The Warning symbol calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning symbol until the indicated conditions are fully understood and met.

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About this edition

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E2466-97007, June 2000

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

A software or firmware code may be printed before the date. This code indicates the version level of the software or firmware of this product at the time the manual or update was issued. Many product updates and fixes do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

The following list of pages gives the date of the current edition and of any changed pages to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed on the title page.